CLAIMS

1. An integrated circuit (IC) comprising:

a processor core operable to perform data processing for the integrated circuit;

a cache memory operable to store data for the processor core; and

an on-chip memory operable to store data for the cache memory, wherein the cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is filled with data from an external memory under user control.

2. The integrated circuit of claim 1, further comprising:

a cache controller operable to handle memory transactions for the cache memory.

3. The integrated circuit of claim 2, further comprising:

a direct memory exchange (DME) controller operable to handle data transfers between the on-chip memory and the external memory.

4. The integrated circuit of claim 3, wherein the DME controller further operates with the cache controller to maintain data integrity for the cache memory.

5. The integrated circuit of claim 2, further comprising:

a direct memory access (DMA) controller operable to handle storage of DMA data received via at least one DMA channel to the cache memory or the on-chip memory.

6. The integrated circuit of claim 5, wherein the DMA controller further operates with the cache controller to maintain data integrity for the cache memory.

7. The integrated circuit of claim 5, further comprising:

a direct memory exchange (DME) controller operable to handle data transfers between the on-chip memory and the external memory, wherein the DME controller couples to the DMA controller via one DMA channel.

8. The integrated circuit of claim 5, further comprising:

an internal memory bus coupling the on-chip memory, the cache controller, and the DMA controller.

9. The integrated circuit of claim 8, wherein the internal memory bus has a width that is equal to a line in the cache memory.

10. The integrated circuit of claim 1, wherein the cache memory and the on-chip memory are fabricated on same integrated circuit die.

11. The integrated circuit of claim 1, wherein the cache memory and the on-chip memory are fabricated on different integrated circuit dies encapsulated within an IC package for the integrated circuit.

12. A wireless apparatus comprising:

an integrated circuit including

a processor core operable to perform data processing,

a cache memory operable to store data for the processor core, and

an on-chip memory operable to store data for the cache memory; and

an external memory operable to store data for the on-chip memory, wherein the cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is filled with data from the external memory under user control.

13. The integrated circuit of claim 12, further comprising:

a direct memory access (DMA) controller operable to handle storage of DMA data received via at least one DMA channel to the cache memory or the on-chip memory.

14. An integrated circuit comprising:

a first processor operable to perform general-purpose processing for the integrated circuit;

a second processor operable to perform data processing for the integrated circuit and including

a processor core operable to perform the data processing, and

a first cache memory operable to store data for the processor core;

an on-chip memory operable to store data for the first cache memory, wherein the first cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is filled with data from an external memory under user control; and

a first memory bus coupling the first and second processors to the external memory.

15. The integrated circuit of claim 14, wherein the second processor further includes a second cache memory operable to store instructions for the processor core, and wherein the second cache memory is filled with instructions from the on-chip memory for cache misses.

16. The integrated circuit of claim 15, wherein the second processor further includes

a first cache controller operable to handle memory transactions for the first cache memory,

a second cache controller operable to handle memory transactions for the second cache memory,

a direct memory access (DMA) controller operable to handle storage of DMA data received via at least one DMA channel to the first cache memory, the second cache memory, or the on-chip memory, and

a direct memory exchange (DME) controller operable to handle data transfers between the on-chip memory and the external memory.

17. The integrated circuit of claim 16, wherein the DMA controller and the DME controller further operate with the first and second cache controllers to maintain data integrity for the first and second cache memories.

18. The integrated circuit of claim 16, wherein the second processor further includes a second memory bus coupling the on-chip memory, the first and second cache controllers, and the DMA controller, and wherein the DME controller couples to the DMA controller via one DMA channel.

19. An integrated circuit comprising a cache controller operable to handle memory transactions for a cache memory and a second memory at two different levels of a cached memory system, the cache controller including

a first address check unit coupled to a first processing unit and operable to determine whether a first memory address for a first memory access by the first processing unit is currently in the cache memory,

a second address check unit coupled to a second processing unit and operable to determine whether a second memory address for a second memory access by the second processing unit is currently in the cache memory, and

a logic unit coupled to the first and second address check units and operable to handle memory transactions for the first and second memory accesses by the first and second processing units.

20. The integrated circuit of claim 19, wherein the logic unit is operable to allow the first processing unit to access the cache memory and the second processing unit to access the second memory, concurrently, if the first processing unit encounters a cache hit and the second processing unit encounters a cache miss.

21. The integrated circuit of claim 19, wherein each of the first and second address check units includes

an address parser operable to parse the first or second memory address to obtain a target tag and a cache line address,

a cache tag RAM operable to provide a stored tag for the cache line address, the stored tag indicating a line in an external memory currently stored in the cache memory at the cache line address, and

a comparator operable to compare the target tag against the stored tag and provide an indication of a cache miss or a cache hit for the first or second memory address.

22. The integrated circuit of claim 21, wherein the first and second address check units are operated independently.

23. The integrated circuit of claim 22, wherein the cache tag RAMs for the first and second address check units are updated concurrently whenever the cache memory is filled with data from the second memory.

24. The integrated circuit of claim 19, wherein the cache controller further includes

a first set of input/output (I/O) ports for interface to the first processing unit, and

a second set of I/O ports for interface to the second processing unit.

25. The integrated circuit of claim 19, wherein the cache memory is a level 1 memory and the second memory is a level 2 memory in the cached memory system.

26. The integrated circuit of claim 19, wherein the second memory is an on-chip memory, wherein the cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is filled with data from an external memory under user control.

27. The integrated circuit of claim 19, wherein the first processing unit is a processor core and the second processing unit is a direct memory access (DMA) controller.

28. A method of handling memory transactions for a cached memory system, comprising:

determining whether a first memory address for a first memory access by a first processing unit is currently in a cache memory;

determining whether a second memory address for a second memory access by a second processing unit is currently in the cache memory; and

allowing the first and second processing units to concurrently access the cache memory and a second memory, respectively, if the first processing unit encounters a cache hit and the second processing unit encounters a cache miss, wherein the cache memory and the second memory are memories at two different levels of the cached memory system.

29. The method of claim 28, wherein the determining for each of the first and second memory addresses includes

parsing the memory address to obtain a target tag and a cache line address,

obtaining a stored tag from a cache tag RAM for the cache line address, the stored tag indicating a line in an external memory currently stored in the cache memory at the cache line address, and

comparing the target tag against the stored tag to determine whether the memory address is currently in the cache memory.

30. The method of claim 29, further comprising:

updating first and second cache tag RAMs, used to determine whether the first and second memory addresses are in the cache memory, whenever the cache memory is filled with data from the second memory.

31. The method of claim 28, further comprising:

if the first and second processing units both encounter cache hits,

selecting one of the processing units to access the cache memory, and

stalling the other processing unit.

32. An apparatus comprising:

means for determining whether a first memory address for a first memory access by a first processing unit is currently in a cache memory;

means for determining whether a second memory address for a second memory access by a second processing unit is currently in the cache memory; and

means for allowing the first and second processing units to concurrently access the cache memory and a second memory, respectively, if the first processing unit encounters a cache hit and the second processing unit encounters a cache miss, wherein the cache memory and the second memory are memories at two different levels of a cached memory system.

33. The apparatus of claim 32, wherein the means for determining for each of the first and second memory addresses includes

means for parsing the memory address to obtain a target tag and a cache line address,

means for obtaining a stored tag from a cache tag RAM for the cache line address, the stored tag indicating a line in an external memory currently stored in the cache memory at the cache line address, and

means for comparing the target tag against the stored tag to determine whether the memory address is currently in the cache memory.

34. The apparatus of claim 33, further comprising:

means for updating cache tag RAMs, used to determine whether the first and second memory addresses are in the cache memory, whenever the cache memory is filled with data from the second memory.